Journal of The Electrochemical Society, **159** (2) H183-H190 (2012)
0013-4651/2012/159(2)/H183/8/$28.00 © The Electrochemical Society

Fabrication of GaAs-on-Insulator via Low Temperature Wafer Bonding and Sacrificial Etching of Ge by XeF_2

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Front end integration of III-V compound semiconductor devices with Si complimentary metal-oxide-semiconductor (CMOS) technology requires the development of commercially viable engineered substrates. The fabrication of engineered substrates currently utilizes technologies such as epitaxy, wafer bonding and layer exfoliation. In this paper we report on the development of GaAs-on-insulator (GaAsOI) structures without the use of Smart Cut technology. Epitaxial GaAs/Ge/GaAs stacks containing an embedded Ge sacrificial release layer were grown with metal-organic chemical vapor deposition (MOCVD) and exhibit both a low defect density as well as surface properties suitable for wafer bonding. A room temperature oxide-oxide bonding process was developed to enable the integration of substrates with a large difference in their coefficients of thermal expansion. The release of the donor substrate and transfer of the GaAs layer onto the handle substrate was realized through room temperature, gas-phase lateral etching of the embedded Ge sacrificial layer by exposure to xenon difluoride (XeF_2). This GaAsOI fabrication process is shown to be successful on a small scale, though implementation for the production of commercially-viable large area GaAsOI substrates at full wafer scale is currently limited by the long gas transport distance associated with a wafer-scale lateral etching process. In order to explore possibilities for overcoming this limitation we established a model that identifies the rate limiting processes and discuss potential approaches that will allow for the implementation of our gas phase lateral etching process for the fabrication of large diameter GaAsOI substrates.
 [DOI: 10.1149/2.070202jes]

Manuscript submitted August 23, 2011; revised manuscript received November 8, 2011. Published December 28, 2011. This was Paper 1951 presented at the Las Vegas, Nevada, Meeting of the Society, October 10–15, 2010.

Developments in engineered substrates have enabled key advancements in many areas of modern microelectronics. For over a decade, Si-on-insulator (SOI) technology has been used in mass production of integrated circuits to reduce transistor leakage current and enhance overall circuit performance. The development of Ge-channel metal-oxide-semiconductor field effect transistors (MOSFETs) and successful demonstration of monolithically integrated III-V compound/Si circuits has prompted the development of Ge-on-insulator (GeOI) substrates and Si-on-lattice-engineered-substrates (SOLES).[1,2] Recently, InAlAs/InGaAs based high electron mobility transistors (HEMTs) and InGaAs/InP based heterojunction bipolar transistors (HBTs) have been fabricated on GeOI substrates and SOLES.[3,4] Each of these engineered substrates: SOI, GeOI, and SOLES, consist of thin layer(s) of high quality semiconductor materials on top of single or multiple oxide layers. Fabrication of such structures is enabled by wafer bonding and layer exfoliation. In recent years, Smart Cut technology has emerged as the most advanced layer exfoliation technique for the fabrication of commercially viable engineered substrates. However, the Smart Cut process is not amenable to all materials combinations due to the requirement of hydrogen implantation[5] and an elevated process temperature window that may generate significant thermal stress when applied to large wafer sizes, particularly in the case of bonded materials with very different coefficients of thermal expansion (CTE).[6,7] Thus, there exists an opportunity for the development of alternative processes that offer more flexibility for materials integration.

Epitaxial lift-off (ELO) processes have been successfully demonstrated in order to create free standing or bonded low aluminum content $Al_xGa_{1-x}As$ epitaxial layers through selective sacrificial etching of embedded high aluminum content $Al_xGa_{1-x}As$ layers with a hydrofluoric acid (HF) solution.[8–11] The ELO approach of transferring a surface layer by selective lateral etching and release has many advantages for engineered substrate fabrication: ELO does not require hydrogen implantation and can be implemented at low temperature ($<300^{\circ}C$), thereby eliminating two of the constraints posed by the Smart Cut process. However, conventional HF-based ELO processes exhibit lateral etch rate limitations due to the inability of the HF to diffuse arbitrary distances to the etch front through the narrow gap created by removal of the sacrificial film. In this process the maximum etch distance and lateral etch rate can be enhanced by physically expanding the separation between the transferred film and donor substrate (through the application of a strained film or via an external mechanical system) in order to enhance diffusion.[11,12]

In contrast with typical HF-based ELO processes described above, we have recently developed an alternative lift-off technique that relies on selective gas-phase etching of an embedded Ge sacrificial release layer. Ge is closely lattice-matched to GaAs, AlAs, and ternary $Al_xGa_{1-x}As$ alloys, but at the same time possesses distinct chemical properties from III-V compound materials. With the proper growth sequence, Ge can be integrated with these materials to produce high quality epitaxial film stacks. It has been demonstrated that the noble gas halide, xenon difluoride (XeF_2), etches Si and Ge with high selectively with respect to III-V semiconductors and commonly used insulators such as SiO_2.[13–15] As described in reference[15] XeF_2 gas etches Ge primarily through the following reaction:

$$Ge(s) + 2XeF_2(g) \rightarrow 2Xe(g) + GeF_4(g) \quad [1]$$

This reaction has an enthalpy of -976 kJ per mole of Ge at 298 K and occurs spontaneously at room temperature.[15] The etchant, XeF_2, and the two most prevalent products, Xe and GeF_4, are in the gas phase at room temperature. Xuan et al. reported a rapid Ge etch rate of 40 μm/min with XeF_2 partial pressure of 0.8 Torr.[13] Previously, we demonstrated a novel XeF_2 based lift-off process and published results estimating the etch selectivity of Ge:GaAs to be on the order of 10^6:1, with linear (non-diffusion limited) etch rates between 30 and 50 μm/min.[15] The rapid etch rates, ability to undercut arbitrary aluminum content $Al_xGa_{1-x}As$ films, high selectivity, and ease of handling post-liftoff (due to the gas-phase nature of the etch) make this XeF_2-based ELO process ideal for the production of freestanding or transferred $Al_xGa_{1-x}As$ heterostructures.

In this work we demonstrate an alternative procedure for fabricating GaAsOI structures by combining our XeF_2-based ELO process with a low temperature oxide-oxide bonding process. We describe in the following sections a path forward for implementing this procedure for the production of engineered substrates with diameters up to

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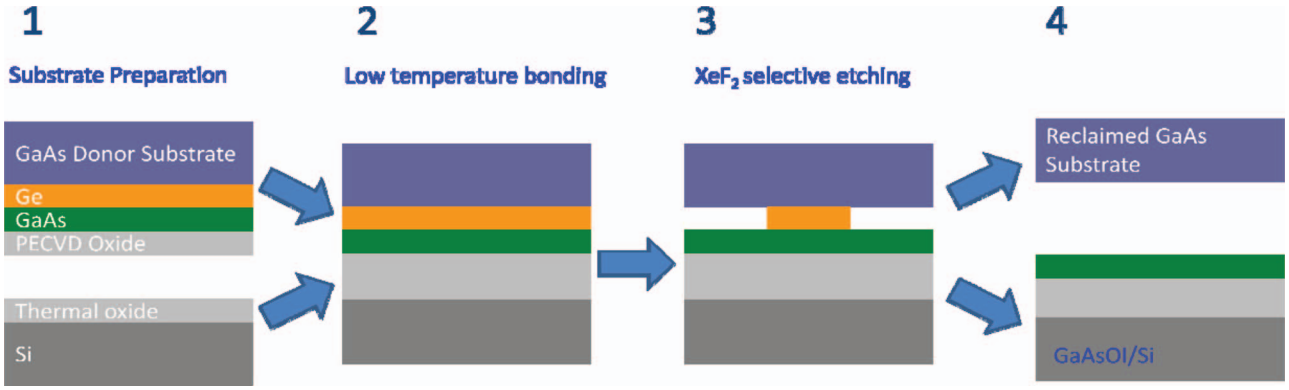

Figure 1. Basic GaAsOI fabrication process demonstrated in this work: 1) Preparation of the bonding substrates: thermally oxidized Si handle wafer and GaAs donor wafer with GaAs/Ge/GaAs epitaxial stack covered with PECVD oxide. 2) Low temperature wafer bonding (room temperature bonding followed by 70°C overnight annealing). 3) Room temperature spontaneous etching with XeF_2 gas in order to selectively remove the sacrificial Ge layer. 4) After separation, GaAsOI on Si substrate and reclaimed GaAs donor substrate.

150 mm, with the key development being the demonstration of small area GaAsOI-on-Si structures.

Fabrication Procedure

Fig. 1 schematically shows our fabrication process. The process consists of three major steps: 1) Bonding substrate preparation, including epitaxial film deposition, oxide deposition and pre-bonding surface treatment, 2) low temperature wafer bonding of the donor wafer with handle wafer, and 3) XeF_2 etching to release and transfer the GaAs thin film on to the handle substrate.

The donor substrates used in this work were AXT manufactured, epi-ready (100) GaAs substrates offcut 6° toward the [011] direction. The GaAs/Ge/GaAs heterostructures were grown with a custom Thomas Swan/AIXTRON low pressure MOCVD system with the capability to deposit Si, Ge, and III-V thin films, thus allowing for the in situ growth of Ge/III-V compound semiconductor heterostructures. For all growths, nitrogen was used as the carrier gas and the chamber pressure was regulated at 100 Torr. The precursors used in this study were GeH_4, AsH_3 and $Ga(CH_3)_3$ (trimethylgallium or TMGa). After epitaxy, the donor wafer was coated with a SiO_2 film that was deposited with an STS plasma-enhanced chemical vapor deposition (PECVD) system. The handle substrate was either a thermally oxidized Si substrate or a quartz substrate. It is important to note that thermally oxidized (or otherwise passivated) silicon wafers are required here in order to avoid attack by XeF_2 during the lateral etching process, as exposed silicon surfaces will spontaneously etch under these conditions. Prior to joining, chemical mechanical polishing (CMP) was used to reduce the PECVD and quartz surface roughness to a level suitable for direct wafer bonding.

The donor and handle wafers were joined at room temperature via direct oxide-oxide bonding, using a commercial EV501 wafer bonder. Either a five minute Piranha clean or an O_2-plasma treatment was used as the pre-bonding activation process. Silicon nitride was deposited on the back-side of the GaAs donor substrate to protect the GaAs during the Piranha clean. The O_2-plasma treatment was carried out in the same STS PECVD system as was utilized for the oxide deposition. After joining, measurements of the bond strength were realized by using a standard gap-opening technique (commonly referred to as a crack opening or razor blade test).

Lateral etching of the embedded Ge sacrificial layer was carried out in two commercial XeF_2 etchers including an SE Tech ES-2000XM XeF_2 etcher and a Xactix Xetch e1 system. In both etching tools, the process followed a charge/etch/pump cycle sequence. A schematic of a typical pulsed etching system as well as a detailed description of the cyclic etching process can be found in Ref. 16. In our experiments, the charging step consists of pressurizing the etching chamber with XeF_2 until the chamber pressure is approximately 2 Torr. As in Ref. 16, the XeF_2 is introduced to the etching chamber through an attached source/expansion chamber. The source/expansion chamber pressure (in this case 3.5 or 4.5 Torr) is generated by the sublimation of a XeF_2 solid source. During the etch step, XeF_2 present in the etch chamber chemically removes exposed Ge. The duration of this step was set to 30 seconds in our process. Following XeF_2 exposure, the etch chamber is evacuated to less than 20 mTorr, removing any unreacted XeF_2 and reaction products in order to prepare the chamber for the next etching cycle. In the ES-2000XM system, throughout the process, a stainless steel disk above the sample rotates at 10 rpm to enhance gas circulation. By the end of the etch sequence the Ge sacrificial layer is consumed and the donor and bonded stack are separated, leaving the epitaxial GaAs layer bonded to the handle substrate, forming a GaAsOI structure. In order to quantify the lateral etch rate, an experiment was performed in the Xactix system (which incorporates an optically transparent etch chamber lid) whereby an automated program was developed to record successive *in situ* images of the etch-front position with a CCD camera, allowing for real-time measurement of the lateral etch propagation. A custom image analysis program written in Mathematica allowed for the generation of plots detailing the etch distance as a function of the XeF_2 exposure time.

Results and Discussion

Growth of high quality Ge/III-V heterostructures.— The growth of a high quality GaAs/Ge/GaAs epitaxial stack is a necessary prerequisite for our GaAsOI fabrication process. Previous reports of GaAs epitaxy on a Ge surface have shown that substrate offcut and the temperature profile during growth are critical parameters for realizing GaAs thin films on Ge that are both free of anti-phase boundaries (APBs) and have a low dislocation density.[17] For the opposite interface, recent results from our group have demonstrated that Ge on GaAs heteroepitaxy initiates properly when the GaAs surface is Ga-rich in nature.[18] Incorporating this knowledge into our GaAs/Ge/GaAs growth procedure has allowed us to successfully fabricate GaAs/Ge/GaAs heterostructures that are APB-free, exhibiting dislocation densities below the transmission electron microscopy (TEM) detection limit and with an RMS surface roughness of ~3 nm over a 10 μm×10 μm area. Fig. 2 shows a cross-section TEM image of a GaAs/Ge/GaAs heterostructure and an AFM image of the surface profile. The surface roughness develops as a consequence of using (100) GaAs substrates offcut 6° toward the [011] direction (note that an offcut toward the [011] direction is crystallographically equivalent to an offcut toward the nearest [111] direction). The substrate offcut toward the [011] direction increases the [0-1$\bar{1}$] ledge density and causes step bunches to form along [0-1$\bar{1}$] direction during growth. The resulting surface morphology is not suitable for direct bonding as this process requires the surface roughness be less than 0.5 nm.[19,20] To overcome this obstacle,

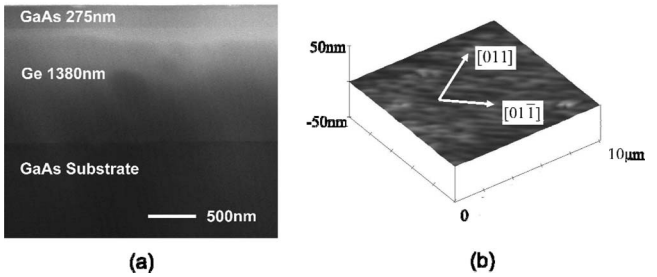

Figure 2. a) XTEM image of a GaAs/Ge/GaAs heterostructure grown on a (100) GaAs substrate with a 6° offcut toward the [011] direction. No anti-phase boundary (APB) was found in the top GaAs layer. b) AFM image of the GaAs surface with formation of step bunches along [0-1$\bar{1}$] direction, leading to RMS roughness of 3.54 nm for a 10 μm by 10μm scan.

a PECVD SiO_2 film was deposited on the epitaxial wafer and CMP was used to smooth the oxide surface to a root-mean-square (RMS) roughness value less than 0.5 nm.

Advantages of our low temperature layer transfer process.— In standard Smart Cut technology, the hydrogen exfoliation process requires the bonded wafer pair to be annealed at an elevated temperature (>300°C) in order to realize H_2 void coalescence and separate the donor substrate from the bonded stack.[21,22] This requirement makes it very difficult to use this process for layer transfer of films from a donor wafer that has a very different CTE, α, from that of the handle substrate. For instance if the bonded wafer pair were to consist of Si ($\alpha_{Si} = 2.6\times10^{-6}$/°C) and GaAs ($\alpha_{GaAs} = 5.73\times10^{-6}$/°C), at elevated temperatures, the strain energy per unit area from the thermal expansion mismatch would likely exceed the bond strength (typical values of a few hundred mJ/m^2) and the wafers would debond or fracture.[6,7] Since our XeF_2 lateral etching process is conducted at room temperature, we eliminate the difficulties associated with thermal expansion mismatch of the bonded wafer pair. The typical oxide-oxide bond strength after room temperature direct bonding is between 50 to 200 mJ/m^2,[19,20] which is sufficient for handling prior to and during the following etch sequence. Once the thin GaAs layer is transferred to the handle substrate, the adverse effects of the CTE disparity is a minor concern as the strain energy resulting from thermal mismatch, which scales with thickness, would be much smaller than the interfacial bond strength. Thus, the final GaAsOI structure can be annealed at high temperature in order to strengthen the oxide-oxide bond for subsequent device fabrication processes.

PECVD oxide layer stress control.— Although CTE mismatch is not a significant obstacle for our process, we have observed that the internal strain energy in the PECVD SiO_2 film can exceed the oxide-oxide bond strength and lead to film delamination. Fig. 3 shows a scanning electron micrograph of a GaAs/SiO_2 film stack transferred to a Si handle substrate that displays a characteristic telephone cord buckling pattern,[23] arising from the high intrinsic compressive stress in the PECVD oxide layer. The strain energy per unit area, E_s, caused by PECVD oxide intrinsic stress can be calculated with the following equation:

$$E_S = \int_0^{h_s} \frac{\sigma_s^2(z)}{M_s} dz + \int_0^{h_f} \frac{\sigma_f^2(z)}{M_f} dz \qquad [2]$$

Here h_s, σ_s, and M_s are the thickness, stress, and biaxial modulus of the handle substrate, while h_f, σ_f, and M_f are the corresponding parameters of the bonded oxide film. The GaAs layer is typically much thinner than the oxide film and has significantly less intrinsic stress, thus it is not considered here. Furthermore, the stress in the handle substrate is negligible, allowing us to ignore the first term in the equation. The failure condition is then determined by the balance between the strain energy in the deposited oxide layer and the oxide-oxide bond strength.

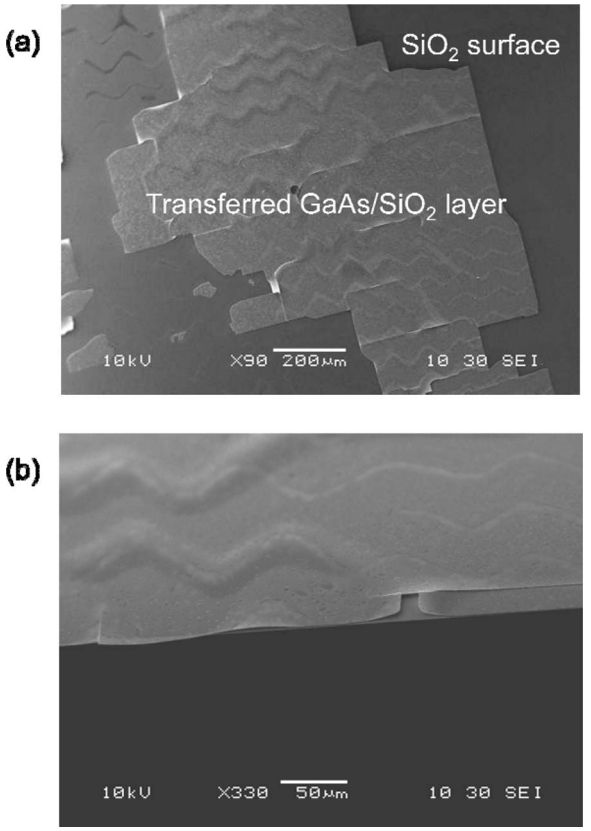

Figure 3. SEM images showing an example of a buckled GaAs/SiO_2 layer after being transferred to the handle substrate, a result of strong intrinsic compressive stress in the PECVD oxide film. a) Top-down view of the transferred film stack. Part of the transferred film peeled off exposing the oxide surface on the handle wafer. b) 37° tilted view of the edge of the sample showing the buckled portion of the GaAs/SiO_2 layer detached from the handle substrate.

As illustrated in Fig. 4, taking the biaxial modulus of PECVD SiO_2 to be 80 GPa, the strain energy in the oxide layer scales linearly with layer thickness, and parabolically with its intrinsic stress. In this case we assume a constant oxide-oxide bond strength of 100 mJ/m^2 (denoted by the green plane in the plot); the bond strength depends on the details of the room temperature direct bonding conditions. When

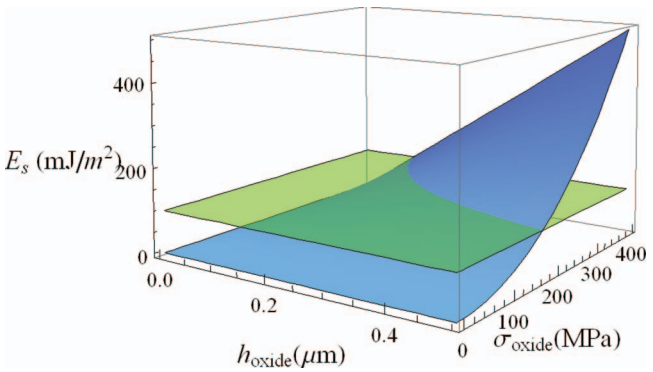

Figure 4. Comparison of strain energy in the PECVD oxide layer (blue surface, plotted against layer thickness, h, and intrinsic stress, σ) and the oxide-oxide bond strength (green plane, assumed to be 100 mJ/m^2 in this example). Once the strain energy exceeds the bond strength the interface will fail, separating the individual components. Improving the probability of a successful bond can be realized by improving the bond strength or reducing both the thickness and internal stress of the oxide layer.

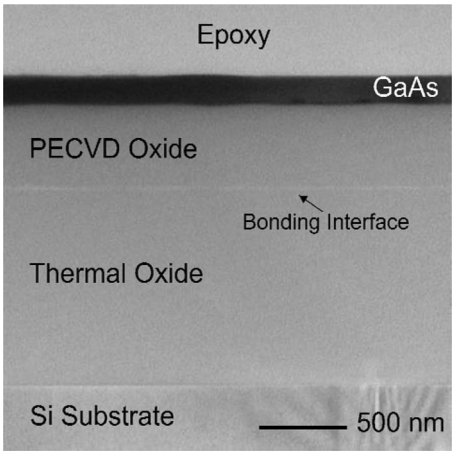

Figure 5. XTEM image demonstrating a high quality GaAsOI/Si structure obtained with our low temperature bonding and gas-phase ELO procedure. Although currently limited to small areas (assuming full thickness wafers are utilized) such heterogeneously integrated structures would be useful for the integration of III-V based optoelectronics devices and HBTs with Si CMOS.

the strain energy (denoted by the blue surface in Fig. 4) exceeds the bond strength, the bond would be expected to fail, whereas when the strain energy is less than the bond strength (shown by the portion of the blue surface below the green plane in the figure), the GaAs/SiO_2 stack would be expected to stay intact.

From this analysis one can see that the probability of successful GaAs layer transfer is maximized by reducing the total strain energy in the oxide film through a reduction in thickness or intrinsic stress, as well as by improving the oxide-oxide bond strength. Under our typical deposition parameters, PECVD derived oxide films tend to display a compressive intrinsic film stress when deposited on Si or GaAs substrates, driven primarily by thermal expansion mismatch. Additional reports have shown the possibility of tuning the stress level within the range of −400 MPa (compressive) to 150 MPa (tensile) by such means as adjusting the reactant gas flow ratio and frequency mixing.[24] Through optimization of the deposition conditions we were able to reduce the compressive stress to 250 MPa, resulting in strain levels low enough to achieve successful bonding. It is important to note that in our current process, the oxide thickness must be a minimum of 100 nm prior to CMP to be able to reduce the surface roughness to a level suitable for bonding. One can also improve the room temperature bond strength by applying a plasma activation process.[25–27] For a GaAs/quartz pair treated with O_2-plasma prior to bonding, we measured a bond strength of ∼70 mJ/m^2 after room-temperature direct bonding. The addition of an annealing step between 60 to 80°C for 14 hours further improved the interfacial bond strength to 240 ± 20 mJ/m^2. At higher annealing temperature the wafer pair was found to delaminate, while annealing for durations exceeding 14 hours showed no further improvement in bond strength. Employing a combination of these methods (oxide film stress reduction and annealing to increase the interfacial bond strength) we have successfully engineered our process to ensure that the GaAs/SiO_2 stack stays bonded to the handle substrate following the XeF_2 etch sequence.

With these improvements incorporated into the process flow, we have successfully fabricated GaAsOI-on-Si samples, verifying the suitability of our low-temperature bonding and gas-phase etching technique for the production of engineered substrates. Fig. 5 shows a cross-sectional TEM image of a typical GaAsOI-on-Si structure fabricated with this procedure, note that the total area of this sample is on the order of 10 mm^2, currently limited by the time required for lateral etching (details to be discussed below). The oxide/oxide bond interface maintained its integrity following processing and can be further strengthened with an annealing step above 700°C making the bonded structure robust for further device fabrication steps.

A model for gas-phase sacrificial Ge etching.— In the sections above we have demonstrated the feasibility of our low temperature fabrication process for the development of small-area GaAsOI samples. However, scaling this process up to large diameter engineered substrates (e.g. 150-mm diameter) requires the realization of rapid centimeter-scale lateral etching of the Ge sacrificial film. We will now discuss the rate limiting mechanisms in our process and propose methods that will allow for the realization of a scalable integration procedure.

The Deal-Grove (D-G) model for oxidation of silicon has been widely adopted for modeling the length dependent etch rate for sacrificial etching of oxide in HF[28,29] and photoresists in acetone.[30] Brazzle et al. first adapted the D-G model to describe XeF_2 etching of silicon.[31] The original D-G oxidation model states that oxide growth rate, R_{ox}, can be modeled by the following equation:

$$R_{ox} = \frac{C^*/C}{\left(\frac{1}{k_{ox}} + \frac{h_{ox}}{D_{ox}}\right)} \quad [3]$$

Here h_{ox} is the thickness of the growing oxide, k_{ox} is the rate constant of the oxidation reaction at the oxide/Si interface, D_{ox} is the diffusivity of the oxidant in the oxide, C^* is the concentration of the oxidant in the oxide at the oxide/air interface, and C is the molar amount of oxidant required for a unit volume of oxide. From Eq. 3, one can see that the oxidation rate is limited by the slower of two mechanisms: (1) the oxidation reaction occurring at the oxide/Si interface or (2) the diffusion of the oxidant through the existing oxide to the oxide/Si interface. At steady state, all parameters except for h_{ox} are constant. As h_{ox} increases, the oxidation rate, R_{ox}, decreases. In other words, the oxidation process slows as it progresses due to the limited diffusion rate of the oxidant through the growing oxide film.

The basic mechanism of our gas-phase sacrificial etching process is similar to the D-G oxidation model. Initially, the etch rate is limited by the reaction of XeF_2 with the exposed Ge. As the etch progresses, transport of the etchant and reaction products to and from the etch front through the narrow channel created by removal of the sacrificial layer eventually limits the rate of undercutting. XeF_2 has a mean free path greater than 10 μm at the average etching pressure of 2 Torr. Since a reasonable Ge sacrificial layer thickness is normally much less than 10 μm, the XeF_2 transport to the etch front is in the molecular flow regime. Brazzle et al. modeled this process as gas transport through a rectangular channel with width w, height h, and length L, and extracted an effective diffusivity D_{eff}, described by the following relation

$$D_{eff} = k_l \left(\frac{w \cdot h}{w + h}\right) \quad [4]$$

where k_l is the mean molecular velocity which for XeF_2 is 139 m/s at 298 K.

With D_{eff}, we can express the lateral etch rate, $\dot{L}$, with a formula that is analogous to the oxidation rate expression in Eq. 3.

$$\dot{L} = \frac{P}{RT} \frac{1}{\left(\frac{1}{k_e} + \frac{L}{D_{eff}}\right) C} \quad [5]$$

Here L is the lateral etching distance, which is also the length of the channel. P is the XeF_2 vapor pressure at the open end of the channel, which we can consider to be the chamber pressure in our case. R is the ideal gas constant, T is the temperature, k_e is the rate constant for the etching reaction, and C is the number of moles of XeF_2 needed to remove one unit volume of Ge, which is equal to 0.1462 mol/cm^3. The P/RT term is the equivalent concentration of XeF_2 at the open end of the channel. As previously described XeF_2 etching is typically carried out in a cyclic fashion where the XeF_2 is replenished in a series of short pulses. The pulsed process is used to ensure that each etching cycle initiates with the same partial pressure of XeF_2.[16] The XeF_2 partial pressure decreases slightly within each etching step as the reaction proceeds. Nevertheless, the etch step duration is typically designed to be short so that the XeF_2 partial pressure drops less than

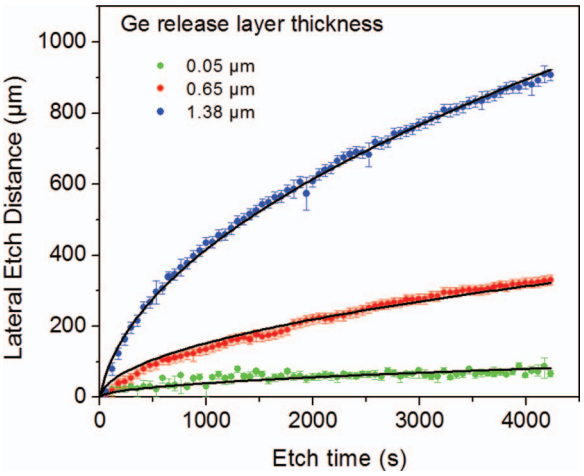

Figure 6. Lateral etch distance vs. etching time for three samples with different Ge layer thicknesses. The black solid lines are curve fits employing Eq. 11, while the points are real-time measurements made in vacuo in the Xactix XeF_2 system. The significant reduction in etch rate with time and Ge layer thickness is apparent from this dataset demonstrating the limitations arising from the use of (planar) full-thickness wafers. The parameters (k_e and k_l) extracted from the fit are used to simulate non-planar etch scenarios.

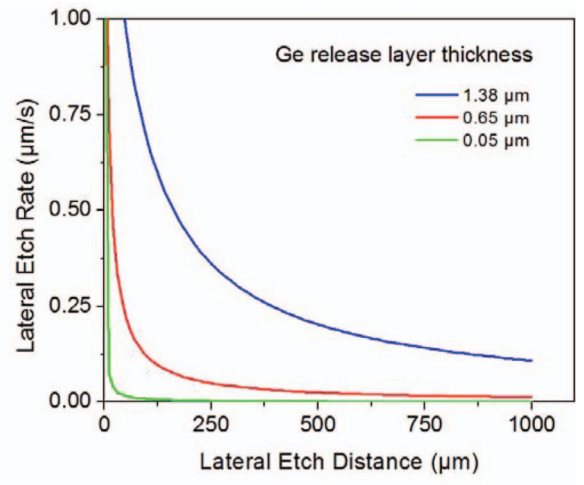

Figure 7. Plot of lateral etch rate vs. lateral etch distance for the three samples presented in Fig. 6, using the parameters extracted from data fitting. The roll-off in etch rate is extremely severe for the 50-nm thick Ge film and, though improved for the thicker layers, does not allow for the undercutting of commercially viable substrate diameters in a realistic time frame.

20 percent. Therefore, as a fair approximation, we can consider *P/RT* term to be constant.

With fixed values for *P/RT* and *C*, the lateral etch rate depends solely on $1/k_e + L/D_{eff}$. At the initial stages of the etch process, *L* is very small resulting in $1/k_e \gg L/D_{eff}$, so the lateral etch rate is a constant and the etch process is in the surface-reaction-limited regime. As the etch progresses, *L* increases and the L/D_{eff} term can no longer be ignored. In the limit that $L/D_{eff} \gg 1/k_e$ the lateral etch rate is constrained by gas transport through the channel, and Eq. 5 can be rewritten as:

$$\dot{L} = \frac{P}{RT} \cdot \frac{1}{C} \cdot \frac{D_{eff}}{L} \qquad [6]$$

Translating our model to the geometry relevant for layer transfer processes, the height of the channel is determined by the embedded Ge layer thickness, *h*, while the width of the channel, *w*, is generally much larger than the sacrificial layer thickness (and is essentially a continuous gap rather than a rectangular channel). With these considerations Eq. 4 can be simplified to the following form:

$$D_{eff} = k_l \cdot h \qquad [7]$$

and Eq. 6 can be rewritten as

$$\dot{L} = \frac{P}{RT} \cdot \frac{k_l}{C} \cdot \frac{h}{L} \qquad [8]$$

Examining Eq. 8, we can see that for a given chamber pressure and temperature, for long lateral etch distances, the etch rate is inversely proportional to the etch depth. This inverse dependence results in a substantial decrease in the sacrificial layer removal rate as the etch front progresses. Fig. 6 shows the measured lateral etch distance as a function of time for three samples with different Ge layer thicknesses. As can be seen in the plot the lateral etch process progresses much slower for thinner Ge layers, as predicted by Eq. 8. For a fixed gap height this imposes a severe limitation for lateral etching processes relevant for the integration of large diameter wafers.

Integrating both sides of the full expression shown in Eq. 5 with respect to the etching time results in the following equation,

$$\frac{\left(L_f^2 - L_i^2\right)}{R_Q} + \frac{\left(L_f - L_i\right)}{R_L} = t_f - t_i \qquad [9]$$

where L_f and L_i are the final and initial etch front positions, at the final and initial times, t_f and t_i respectively. Parameters R_L and R_Q are the linear and quadratic rate constants, with units of µm/s and µm²/s, and can be expressed as the following:

$$R_L = \frac{P \cdot k_e}{R \cdot T \cdot C}; \quad R_Q = \frac{2 \cdot P \cdot k_l \cdot h}{R \cdot T \cdot C} \qquad [10]$$

Taking t_i and L_i as zero we solve Eq. 9 for L_f to yield the position of the etch front as a function of time.

$$L_f = k_l \cdot h \cdot \left(\frac{-1}{k_e} + \sqrt{\left(\frac{1}{k_e}\right)^2 + \frac{P}{R \cdot T} \cdot \frac{2 \cdot t_f}{C \cdot k_l \cdot h}} \right) \qquad [11]$$

Eq. 11 allows us to calculate the lateral etch distance for a given etch duration using only physically relevant parameters. Additionally, this expression enables simple fitting of the measured lateral etch distance data, shown as black lines in Fig. 6 for the three samples with varying Ge layer thicknesses. As discussed above, among the parameters in Eq. 11, *P/RT* and *C* are constants, and *h* was fixed by TEM measurements. Only the mean molecular velocity, k_l and etch reaction rate constant, k_e are not directly measurable and are thus chosen to be fitting parameters.

The fitted value of k_e is 2.5 m/s, and k_l is 124.1, 29.3, 24.1 m/s for the samples with 1.38, 0.65, 0.05 µm Ge layers respectively. k_e at 2.5 m/s corresponds to a linear etch rate of 1.685 µm/s, which is consistent with previous measurements of the bulk etch rate. The extracted k_l of 124.1 m/s for the 1.38 µm sample is close to the theoretical value 139 m/s for XeF_2. We believe that the reduced mean molecular velocity for samples with thinner Ge layers is due to increased probability of collisions with the channel ceiling and floor in these confined structures, resulting in a decrease in the overall molecular kinetic energy. The excellent match between theory and experiment displayed in Fig. 6 proves that our modified D-G model captures the essential physics present in this etching process. With the extracted parameters, the model can now be used to provide guidance for further experimental development.

Using the fitted values of k_e and k_l, we can plot the decrease of the lateral etch rate as the etch progresses for the three measured samples (Fig. 7). Consistent with the model, the lateral etch rate decreases dramatically for samples with a thinner Ge sacrificial layer. Extrapolating from the fitted data set we estimate that an etching time of >200 days is required to release a full 150-mm diameter wafer (assuming a Ge sacrificial layer thickness of 1.38 µm), which is obviously not a practical option for the transfer of an epitaxial film. Therefore we must consider modifications to our current process in

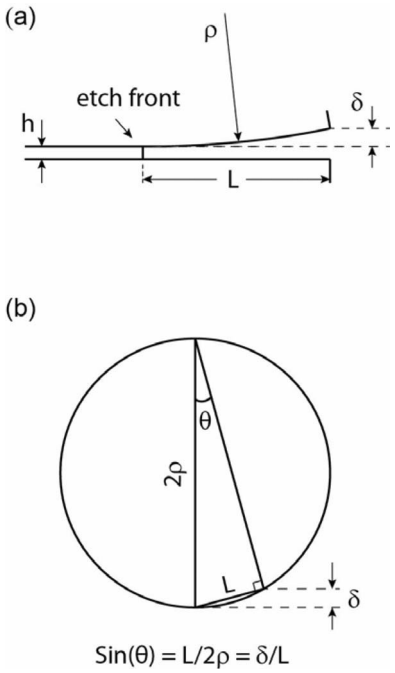

Figure 8. a) An illustration of gap opening during the lateral etch process. The additional curvature (described by a radius of curvature ρ), increases the effective gap size by δ over the length of the etch front, *L*. b) Detailed geometry showing the relation between *L*, ρ, and δ.

order to make this technique viable for the fabrication of commercially relevant large-area engineered substrates.

Potential methods to extend the lateral etch limit.— The analysis above assumed that the channel height was fixed by the thickness of the Ge film. In practice however, the channel height does not have to coincide with the initial sacrificial layer thickness. As illustrated in Fig. 8a, the released section of the substrate pair can bend away from the bonded interface in order to create an additional displacement of δ, yielding a total channel height of $h+\delta$ at the open end. Under these conditions the effective diffusivity varies along the lateral etch direction. At the open end of the channel the diffusion would be significantly improved, while close to the etch front the effective diffusivity is still limited by *h*. In this configuration the overall gas transport through the channel will be enhanced and the overall etch rate would increase.

Such a scenario has previously been experimentally investigated in the development of liquid-phase HF-based ELO processes for the transfer of large area devices such as solar cells to arbitrary handle substrates.[9,11,12,32,33] Several different methods to expand the channel have been demonstrated. The first method pioneered by Yablonovitch et al. (implemented in liquid-phase HF-based ELO processes) was the use of a tensile strained wax layer to cause the released section of the thin epitaxial film to curve up and thus increase the effective gap height.[9] This method is limited to thin released layers due to the relatively low stress imparted by the wax. In order to further enhance the maximum achievable etch rates, a weight induced separation process has also been demonstrated.[12] In this method, the donor substrate is bonded face-down onto a flexible carrier substrate. The stack is then mounted to the bottom of a supporting rod and submerged in an HF solution with a weight attached to one side of the flexible carrier. As the etch progresses the weight pulls one end of the flexible carrier downward, opening the gap and increasing the channel height and thus enhancing the lateral etch rate. Recently, Schermer et al. further increased the lateral etch rate by employing a support cylinder to apply a constant curvature to the flexible carrier.[11,33]

In Ref. 9, Yablonovitch et al. outlined a mathematical model for this scenario and worked out the lateral etch rate of AlAs by a dilute HF solution when a fixed curvature is applied to the lifted film. Following the steps outlined in Ref. 9, we now explore the enhancement in etch rate arising from the application of a fixed curvature on the released structure for our gas-phase etching technique.

First, for the case without gap opening discussed above, when the etch rate is limited by diffusion, equating diffusion flux with chemical reaction flux at the etching front, we obtain:

$$\dot{L}hC = \frac{D_{eff}h}{RT}\cdot\frac{dP}{dz} = \frac{k_l h^2}{RT}\cdot\frac{dP}{dz} \qquad [12]$$

where *z* is the position coordinate along the channel and *dP/dz* is the pressure gradient. In Ref. 9, the rate limiting mechanism was diffusion of the etching product, H_2 gas, in the dilute HF solution, and the diffusivity was assumed to be a constant. For our gas phase etching process, as discussed above, the effective diffusivity depends on the gap size as it is controlled by the channel conductance, in this case determined by the Ge layer thickness, *h*. Integrating Eq. 12 along a channel with length *L* results in an expression for the lateral etch rate, identical in form to Eq. 8, as discussed previously.

When a fixed curvature is applied to one side of the channel, as illustrated in Fig. 8a, the gap height at any point along the channel can now be expressed as $h+\delta$. Examining the geometry illustrated in Fig. 8b, we see that at the open end of the channel $\delta/L = L/2\rho$, where ρ is radius of curvature of the deformed structure. This relation also holds for any give point along the channel, where $\delta/z = z/2\rho$, with $z = 0$ representing the instantaneous etch front position.

Taking this into account, Eq. 12 can now be written as

$$\dot{L}hC = \frac{k_l}{RT}\cdot\left(h+\frac{z^2}{2\rho}\right)^2\cdot\frac{dP}{dz} \qquad [13]$$

Following the procedure outlined in Ref. 9 we integrate Eq. 13 from zero (the etch front position) to infinity, and find:

$$\dot{L} = \frac{P}{RT}\cdot\frac{k_l}{C}\cdot\frac{2}{\pi}\cdot\sqrt{\frac{2h}{\rho}} \qquad [14]$$

This equation shows that even for the worst case scenario where the channel is infinitely long, by employing a fixed curvature, the lateral etch rate maintains a constant minimum value, which scales as the square root of the sacrificial Ge layer thickness and inversely with the square root of the radius of curvature of the gap. In other words, employing a thicker Ge layer and applying a tighter curvature would increase the minimum lateral etch rate. To illustrate this dependence, Fig. 9 shows the minimum XeF_2 lateral etch rate at different fixed channel radius of curvature for Ge layer thickness of 1 μm, 2 μm, and 5 μm, as calculated from Eq. 14.

Comparing this expression with Eq. 4 from Ref. 9, we can see that in the case of gas phase XeF_2 etching, a larger Ge thickness enables more rapid etching, whereas in conventional liquid phase ELO an inverse thickness dependence results in expedited etching for very thin sacrificial layers. For our gas-phase process this opposite dependence arises from the fact that the effective diffusivity of XeF_2 (determined by the hydraulic conductance of the gap) depends directly on the channel height (Eq. 7 above). In both cases, the lateral etch rate is inversely proportional to the square root of ρ. By employing a smaller ρ (tighter curvature), it is possible to realize a significant reduction in the required etching time.

It is important to point out that, though slow, our standard (fully planar) process for the fabrication of engineered substrates utilizes the direct bonding of full-thickness wafers followed by the release and transfer of the desired film to the host substrate without requiring the modification, or in more extreme cases, the destruction of the donor wafer. Such a procedure allows for significant cost savings through reuse of the original epitaxial growth substrate. However, with these constraints, the released structure is significantly more rigid and less amenable to generating a tight radius of curvature. A typical 500-nm thick silicon nitride film with 400 MPa tensile strain deposited

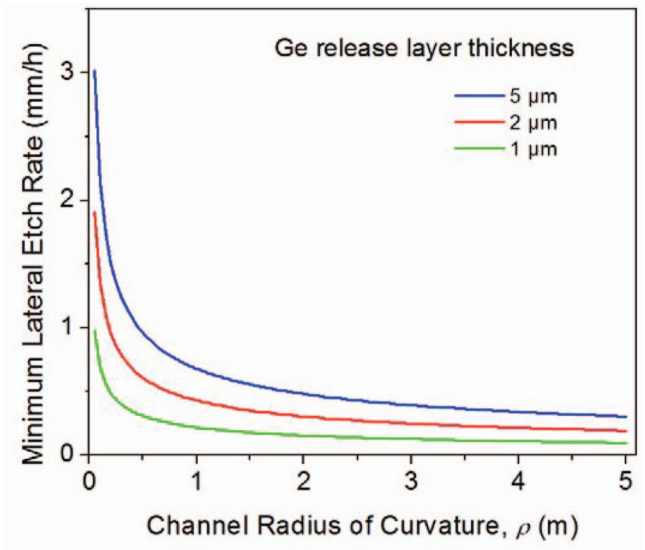

Figure 9. Minimum lateral etch rate vs. radius of curvature of the channel, for Ge layer thicknesses of 1, 2, and 5 μm. As opposed to the continuously decreasing rate observed for planar structures, a constant minimum etch rate can be realized for a bonded structure with an imparted curvature. Such a procedure allows for a significant reduction in the required release time, increasing the maximum wafer diameter that can be released for a given etch time.

on a 0.65-mm-thick GaAs substrate is only able to generate a curvature with radius of about 40 m. By moving to a 1 GPa film of 2 μm thickness, the generated radius of curvature would be reduced to about 4 m. From Fig. 9, we can see that an imposed radius of curvature of 4 m combined with a Ge release layer thickness of 5 μm would give a minimum lateral etch rate about 0.35 mm/h. With this rate, a 150-mm diameter wafer (requiring a lateral etching distance of 75 mm for release) can be undercut in about 215 hours. Although this is a significant improvement over the previous result (which required etching times approaching one year) this process is still too slow to be commercially viable.

Although further reductions in the etching time can be realized through increases in the Ge thickness, limitations in the maximum epitaxial film thickness may preclude sacrificial layer thicknesses beyond 20 μm. In theory, employing a thicker stressed film with a higher tensile stress level would generate tighter curvature. However in practice the high stress level would likely fracture the substrate or lead to delamination of the bonded pair.

Mechanical thinning of the donor substrate prior or after bonding would make it more amenable to generating a tight radius of curvature. Reducing the thickness of the GaAs donor substrate to 50 μm would reduce the radius of curvature generated by a 400 MPa, 500-nm thick silicon nitride film to 0.258 m resulting in a release time of about 60 hours for a bonded 150 mm wafer stack; note that the required time scales linearly with wafer diameter, so for this example a 2-inch diameter wafer could be released in only 20 hours. The drawback of this approach is that the lapping process excludes the re-use of the donor substrate.

Utilization of a temporary flexible transfer substrate (followed by post release bonding of the transferred film) would enable even tighter curvature for a viable XeF_2-based ELO process and reuse of the donor substrate. Although it introduces additional complexity to the process, moving away from a rigid full-thickness substrate would enable the use of physical means to significantly widen the channel in order to enhance the gas transport through the narrow gap defined by the sacrificial layer. It is interesting to point out that the implementation of such a system is also viable for our approach and should be straightforward to implement owing to the simplicity of the gas-phase etching system. With a compliant backing it should be possible to achieve a radius of curvature of 0.05 m (similar to that used by Schermer et al[11,33]), significantly reducing the required etch time to about 25 hours for layer transfer over a full 150-mm diameter wafer (compared with 8 hours for a 2-inch diameter substrate).

Conclusions and Future Work

We have developed and thoroughly investigated a novel low temperature process for the fabrication of GaAs-on-insulator (GaAsOI) structures. This technique relies upon room temperature oxide-oxide bonding in combination with a gas-phase XeF_2-based selective Ge lateral etching process. The GaAs/Ge/GaAs epitaxial structures were fabricated via MOCVD with the embedded Ge film serving as a sacrificial release layer. Employing this procedure we have demonstrated the successful development of high quality GaAsOI-on-Si structures over a small area and find that implementation of this process on a commercially-viable wafer scale is currently impractical due to kinetic limitations of the gas-phase lateral etching process. The rate limiting step was found to be the reduced mass transport of etchant and reactant species through the narrow gap created by the removal of the Ge release layer. We adapted the Deal-Grove oxidation model in order to establish a model describing the relationships between the lateral etch rate, lateral etch distance, release layer thickness, channel displacements, and the radius of curvature of the donor wafer. From these expressions we find that channel opening methods are critical for implementing lateral sacrificial etching techniques for large area layer transfer. Finally, we have proposed possible approaches to extend our procedure for the successful fabrication of GaAsOI engineered substrates, with 2-inch diameter transferred wafers requiring 8 hours for successful film transfer and 150-mm diameter wafers requiring 25 hours of total etching.

Acknowledgments

This work was supported by the Singapore-MIT Alliance (SMA). The fabrication was carried out at the Microsystems Technology Laboratory (MTL) at MIT. This work made use of the MRSEC Shared Experimental Facilities at MIT, supported by the National Science Foundation under award number DMR-08-19762. G.D.C. is a recipient of a Marie Curie Fellowship of the European Commission.

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